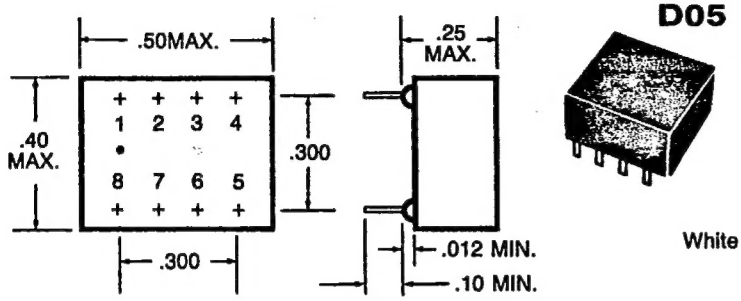
DIL•DIP AND SURFACE MOUNTING DIGITAL DELAY LINES TTL COMPATIBLE 8 PIN PACKAGE

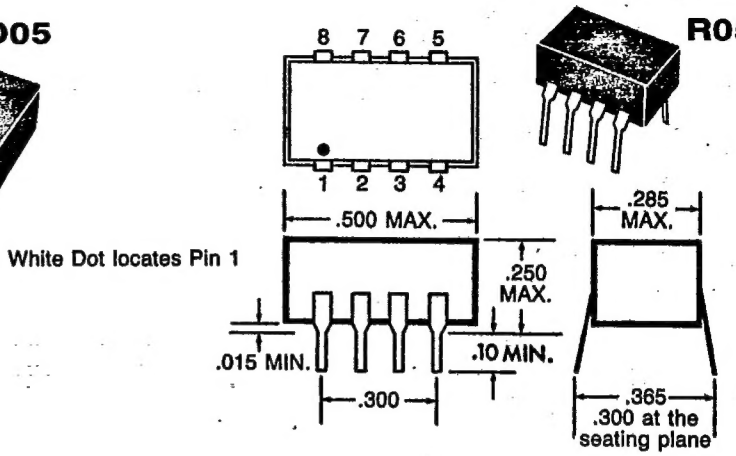
YCL

SERIES D05, R05 AND SSM-5TAPS

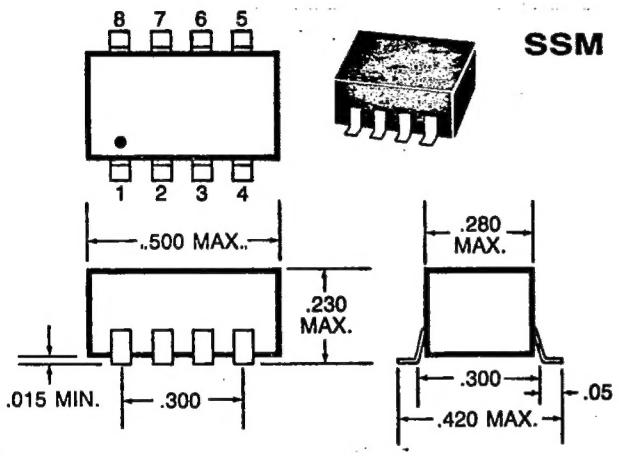


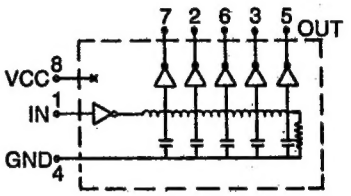
D05

R05



SSM





MODEL NO.			TOTAL DELAY (ns)	DELAY TAP (ns)
SERIES D05	SERIES R05	SERIES SSM		
D05025	R05025	SSM-05025	25	5
D05030	R05030	SSM-05030	30	6
D05040	R05040	SSM-05040	40	8
D05045	R05045	SSM-05045	45	9
D05050	R05050	SSM-05050	50	10
D05075	R05075	SSM-05075	75	15
D05100	R05100	SSM-05100	100	20
D05125	R05125	SSM-05125	125	25
D05150	R05150	SSM-05150	150	30
D05200	R05200	SSM-05200	200	40
D05250	R05250	SSM-05250	250	50
D05300	R05300	SSM-05300	300	60
D05400	R05400	SSM-05400	400	80
D05500	R05500	SSM-05500	500	100

DC PARAMETERS		LIMITS	
		Min.	Max.
Voh	Vcc = min Ioh = 1.0mA	2.5V	—
Vol	Vcc = min Iol = 20mA	—	0.5V
Iih	Vcc = max Vih = 2.7V	—	50μA
Iil	Vcc = max Vil = 0.5V	−2.0mA	—
Ii	Vcc = max Vi = 5.5V	—	1.0mA
Vi	Vcc = min Iin = −18 modc	−1.2vdc	—
Icc	Vcc = max outputs low	—	70mA

SPECIFICATIONS:

- Supply voltage: 5.0VDC ± 10%
- Delay tolerances: ±2ns or ±5% wig
- Minimum pulse width: 40% of Total Delay
- Maximum duty cycle: 50%
- Rise time: 4ns max
- Operating temp. range: 0°C to +70°C
- Temp. coeff. of delays: 1.0ns +500ppm/°C
- Terminals: .020w × .010th., alloy 42

TEST CONDITIONS:

- Vcc = 5.0VDC, Temp. 25°C ± 5°C
- Time delay measured at the 1.5V level
- Rise time measured from .75V to 2.4V
- All outputs loaded with 15pf
- Input Test Pulse:
  - Pulse Voltage: 3.0V
  - Pulse rise time: 2ns
  - Pulse width: 1.2 × max Td
  - Pulse spacing: 5 × max Td